## REMARKS

This is in response to a non-final Office Action dated May 10, 2004. Applicant respectfully traverses and requests reconsideration.

**Rejection under 35 U.S.C. §103**

Claims 20 through 32 are rejected under 35 U.S.C. §103(a) based on Benjamin Clifton et al., U.S. Patent No. 6,388,648 (Clifton), and further in view of Curtis Priem, U.S. Patent No. 5,805,175 (Curtis).

**Clifton**

Clifton is directed to color gamma luminance matching technique for use with an image display system. (Clifton, title.) More specifically, Clifton discloses utilizing a plurality of LCD projection units having luminance and color balance systems employing an LCD array characterization lookup table storing multiple sets of luminance and gamma correction values selectable to control luminance and color balance. (Clifton, abstract.) Color gamma correction systems are combined with luminance and color balancing systems to match primary colors in addition to white and luminance values. The combined systems provide suitable color matching for an image, solving problems associated with a multiscreen display system. Using a color mixing method, primary colors are adjusted and a primary color matching algorithm involves measuring intrinsic color coordinates of primary colors, for determining a set of predetermined target coordinates and performing matrix operations to calculate the set of coefficients used in a color space conversion circuit to convert measured to target coordinates, thereby matching primary colors. (*See e.g.,* col. 3, lines 33-39.)

**Priem**

Priem is directed to a method for providing a plurality of color formats from a single frame buffer. (Priem, title). As shown in FIG. 2, graphics output display circuitry 17 includes a frame buffer 25, which may be used to store the pixel data to be presented on the output display device 18. (Priem col. 5, lines 64-66.) FIG. 5 includes a frame buffer 25 arranged to store data

in the various pixel patterns described. (Priem col. 11, lines 60-61.) Means 41 (rendering device as shown in FIG. 5) is provided for transferring data to the frame buffer in accordance with the depth of the frame buffer selected and the color mode of the application program. (Priem col. 11, lines 61-64.) Means 43 is illustrated for refreshing and reading data from the frame buffer in the appropriate patterns depending on the depth of the frame buffer and the color mode of the application. (Priem col. 12, lines 2-5.) Also shown in FIG. 5 are lookup tables 47, digital-to-analog conversion circuitry 27, and circuitry connecting to those circuits from the frame buffer. (Priem col. 12, lines 17-19.) This latter circuitry includes a first set of multiplexors 46, which are controlled by the value of the decode bit held in the storage means 45 for selecting whether bits are transferred from the frame buffer to the lookup tables in a single group or in three individual groups. (Priem col. 12, lines 20-24.) The connecting circuitry also includes a second set of three multiplexors 48 controlled by the lookup/bypass bit stored with the pixel values in the frame buffer for selecting whether pixel values transferred straight from the frame buffer 25 or pixel values provided by the lookup tables are transferred to the DAC 27. (Priem col. 12, lines 24-29.)

**Independent Claims 20 and 21**

The Office Action acknowledges that "Clifton fails to specifically disclose receiving the display information from the frame buffer [25]." (Office Action p. 3, lines 9-10.)

Claims 20 through 21 recite, *inter alia*, "a frame buffer, wherein the frame buffer stores display information;" and "the gamma correction block receives the display information from the frame buffer." In support of the present rejection, the Examiner asserts that "Clifton discloses a frame buffer storing display information (FIG. 2)." (Office Action p. 2, para. 2, 2d sentence.) FIG. 2 of Clifton illustrates a video signal source 14, multiscreen display driver 16, multiple display controllers 18A-18N and multiple displays 12 within a multiscreen display. Furthermore, the complete discussion of FIG. 2 of Clifton consists of 17 lines of text, as follows:

> FIG. 2 shows an exemplary multiscreen display system 10 employing a three-by-three array of LCD projection units 12A, 12B, . . . to 12N (collectively LCD projection units 12). Of course, N may be as small as two and as big as practical to form a very large array of LCD projection units. Of course, this

> invention may also be employed in stand-alone LCD units. A conventional video signal source 14 drives a conventional multiscreen display driver 16, such as the PICBLOC 3 unit described in the backgroumd section of this application. Each of LCD projection units 12 are interconnected with multiscreen display driver 16 by associated display controllers 18A, 18B, . . . , to 18N, which perform LCD projection unit luminance and color balance functions as described below with reference to FIGS. 4-10. Display controllers 18 are preferably integrated within projection units 12. Multiscreen display system 10 seamlessly displays a total image having a substantially uniform luminance and color balance.

FIG. 2 and the accompanying text of Clifton disclose a video signal source providing an incoming video signal to a driver 16 that divides the signal into appropriate subsignals for the various display controllers 18. Clifton discloses a completely different system from the present claims, subdividing a display for multiple LCDs, and generates a completely different result that does not teach, among other things, including a frame buffer to store the display information prior to performing gamma correction thereon. Applicants are unable to find where FIG. 2 illustrates a frame buffer storing display information as arranged in the claims. Further, the Applicants are unable to find where Clifton as cited discloses a frame buffer storing display information. It should also be noted that none of the further figures and specification of Clifton appear to disclose the claimed frame buffer of claims 20 through 21. Therefore, it is submitted the rejection is improper, as Clifton fails to disclose all of the claimed limitations.

As to the cited Clifton language, which states:

> In this embodiment, 8 bits each of R, G, and B digital input data are received from multiscreen display drivers 16. A lookup table 100 stores the sets of gamma corrected data values described above. A controller 101, such as the above described processor, is employed to manually or automatically select from among the lookup tables. Lookup table 100 receives the R, G, and B digital input data and converts it to corrected data values in accordance with the selected set of lookup table values. A DAC 102 receives the corrected data values and provides corresponding voltages that are conditioned by an LCD driver amplifier 104 into R, G, and B input voltages received by an LCD array 40.

(Clifton col. 10, lines 16-30.) As previously stated, the Office Action acknowledges that Clifton fails to specifically disclose receiving the display information from the frame buffer 25.

(Office Action p. 3.) According to the Office Action, Priem discloses, in FIG. 2, a reference "25" as the cited claim language that Clifton fails to disclose. However, FIG. 2 (reference 25) simply refers to a frame buffer coupled to bus 12 and DAC 27 via 19. The Office Action fails to show where the combination of Priem and Clifton describes, among other things, "wherein the gamma correction block receives the display information from the frame buffer 25." Further, the Office Action fails to show where Priem describes a gamma correction block. The Office Action further fails to show where in Priem the gamma correction block receives the display information from the frame buffer 25. Consequently, the Office Action ignores, among other things, a principal limitation of the claims, namely, "wherein the gamma correction block receives the display information from the frame buffer and gamma selection information."

The Office Action asserts Priem teaches transferring data from the frame buffer 25 to the lookup tables, citing column 12, lines 21 through 30. However, the cited portion of Priem, which states, "This latter circuitry includes the first set of multiplexors 46, which are controlled by the value of the decode bit held in the storage means 45 for selecting whether bits are transferred from the frame buffer to the lookup tables in a single group or three individual groups," is limited to multiplexors for selecting whether bits are transferred from the frame buffer 25 to the lookup table, in merely "a single group or three individual groups," rather than, "wherein the gamma correction block receives the display information from the frame buffer 25 and gamma selection information."

According to the Office Action, "It would have been obvious to one of ordinary skill in the art to incorporate Priem's receiving the display information from the frame buffer [25] with the disclosure of Clifton to provide a specific source from which to retrieve pixel data of the video source signal, which he processes to display corrected image data." However, Clifton already describes providing a specific source, namely, "8 bits each of R, G, and B digital input data are received from multiscreen display drivers 16," rather than, "wherein the gamma correction block receives the display information from the frame buffer 25 and gamma selection information." Accordingly, Clifton teaches away from the claims, and, therefore, one would not

be motivated to modify Clifton in a manner as suggested in the Office Action.[1] The Office Action, therefore fails to establish insufficient motivation for one skilled in the art to modify Clifton, and, as a result, the Office Action fails to establish a *prima facie* case of obviousness.

Further, the Office Action provides no support for the assertion that the use of a ball grid array package could be used for "increasing a bond strength between the packaged semiconductor and the substrate." Additionally, the Office Action fails to specify what the ball grid array increases the bond strength with—i.e., does the ball grid array increase bond strength relative to bond wires? If so, no support for such an assertion is provided, and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

Measuring a claimed invention against the standard established in §103 requires the difficult but critical step of casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field.[2] Close adherence to this methodology is especially important in the case of less technologically complex inventions, where the very ease with which the invention can be understood may prompt one "to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher."[3]

The showing of such a suggestion, teaching or motivation must be clear and particular.[4]

**Independent Claim 22**

The Office Action acknowledges that Clifton fails to specifically disclose the pixel information as generated from the display information within a frame buffer. (Office Action p. 4, lines 8-10.) Regarding claim 22, Applicant resubmits the above position regarding claims 20

[1] A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983). *See* M.P.E.P. §2141.02.
[2] *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).
[3] *Id.*
[4] *Dembiczak*, 50 U.S.P.Q.2d 164, 167 (Fed. Cir. 1999); *See, e.g., C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352, 48 U.S.P.Q.2d 1225, 1232 (Fed. Cir. 1998).

and 21, especially since claim 22 recites "pixel information is generated from display information stored within a frame buffer." As noted above, Clifton does not disclose a frame buffer and therefore does not disclose the pixel information generated from display information stored within the frame buffer. Priem, as cited at column 12, lines 22 through 23, is limited to "bits transferred from the frame buffer to the look up tables,. . ." rather than, "wherein the pixel information is generated from display information stored within a frame buffer." Therefore, for at least the same reasons as noted above with regard to claims 20 and 21, it is submitted the present rejection is improper and should be withdrawn.

**Claims 23 through 32**

Regarding claims 23 through 32, it is submitted that these claims contain further patentable subject matter in view of Clifton. Applicant respectfully resubmits at least the above-offered reasons regarding claims 20 and 21 and submits that claims 23 through 32 add further claimed limitations not disclosed by Clifton. Further, claims 28 through 32 add additional claimed limitations not disclosed by Clifton. For example, claims 23 and 28 recite limitations to the claimed gamma correction block, wherein the gamma correction block receives display information from the frame buffer. Regarding claims 27 and 32, Priem, as cited, teaches reading the frame buffer during the refresh process, rather than, "wherein the gamma correction tables are memory structures addressed by the received input data." As noted above, Clifton does not disclose, *inter alia*, a frame buffer and therefore does not disclose all of the claimed limitations. On these grounds, reconsideration and withdrawal of the present rejection is respectfully requested.

**Conclusion**

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and that a early Notice of Allowance be issued in this application. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: August 10, 2004

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